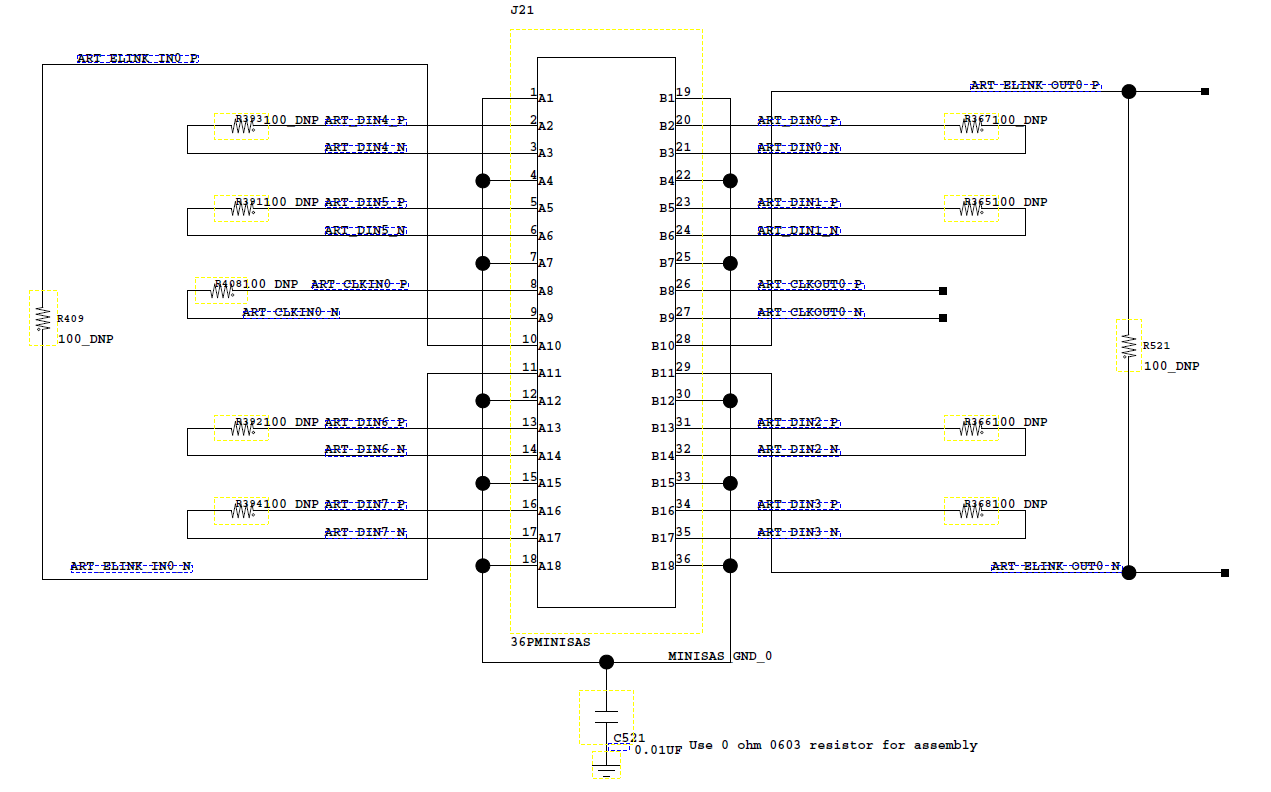
ADDC V1 notes:

Data inputs from MMFE-8:

J21~J24 on ADDC boards, ref to the picture below:



ART\_DIN\_\* diff pairs are used to receive ART data. In current firmware the ART\_CLKIN\_0 clock (160MHz) are used to drive all the data from all 4 MiniSAS connectors. All the ART\_ELINK\_\* pairs LIN\_OUT pairs are NOT connected to any FPGA firmware ports.

The ART signals are transmitted in 8-bit frame under 160 MHz DDR mode (320Mbps). Each frame starts with a flag bit ‘1’, followed by a bit ‘0’ and then 6-bit ART addresses, so total 8 bits in 25 ns.

In FPGA the IO standards for ART signals input pins are LVDS\_25 with internal terminations. It could work well with the SLVS interface (200 mV +/- 200mV), for the VMM custom LVDS we didn’t test it yet.

Data outputs:

Please refer to the table below, at every 40MHz clock cycle a 112-bit GBT frame will be sent to the MM Trigger Processor, if no incoming ART data during this clock cycle then all the bits are ‘0’ except the beginning “1010” flag and BCID counters. If any channel has input then it will be recorded. In one clock cycle, all the channels that have input ART data will be recorded in the 32-bit “Hit List” but only up to 8 ART addressed will be recorded.

|  |  |  |
| --- | --- | --- |
| **GBT Data Bits** | **Signal** | **Notes** |
| 111:110 | “1010” |  |
| 107:96 | BCID |  |
| 95:88 | Error flags |  |
| 87:56 | Hit List | The least significant bit in the hit list corresponds to the inner radius VMM |
| 55:50 | ART Data 7 |  |
| 49:44 | ART Data 6 |  |
| 43:48 | ART Data 5 |  |
| 37:32 | ART Data 4 |  |
| 31:26 | ART Data 3 |  |
| 25:20 | ART Data 2 |  |
| 19:14 | ART Data 1 |  |
| 13:8 | ART Data 0 | ART Data 0 corresponds to the least significant hit bit in the hit list |
| 7:0 | Parity |  |